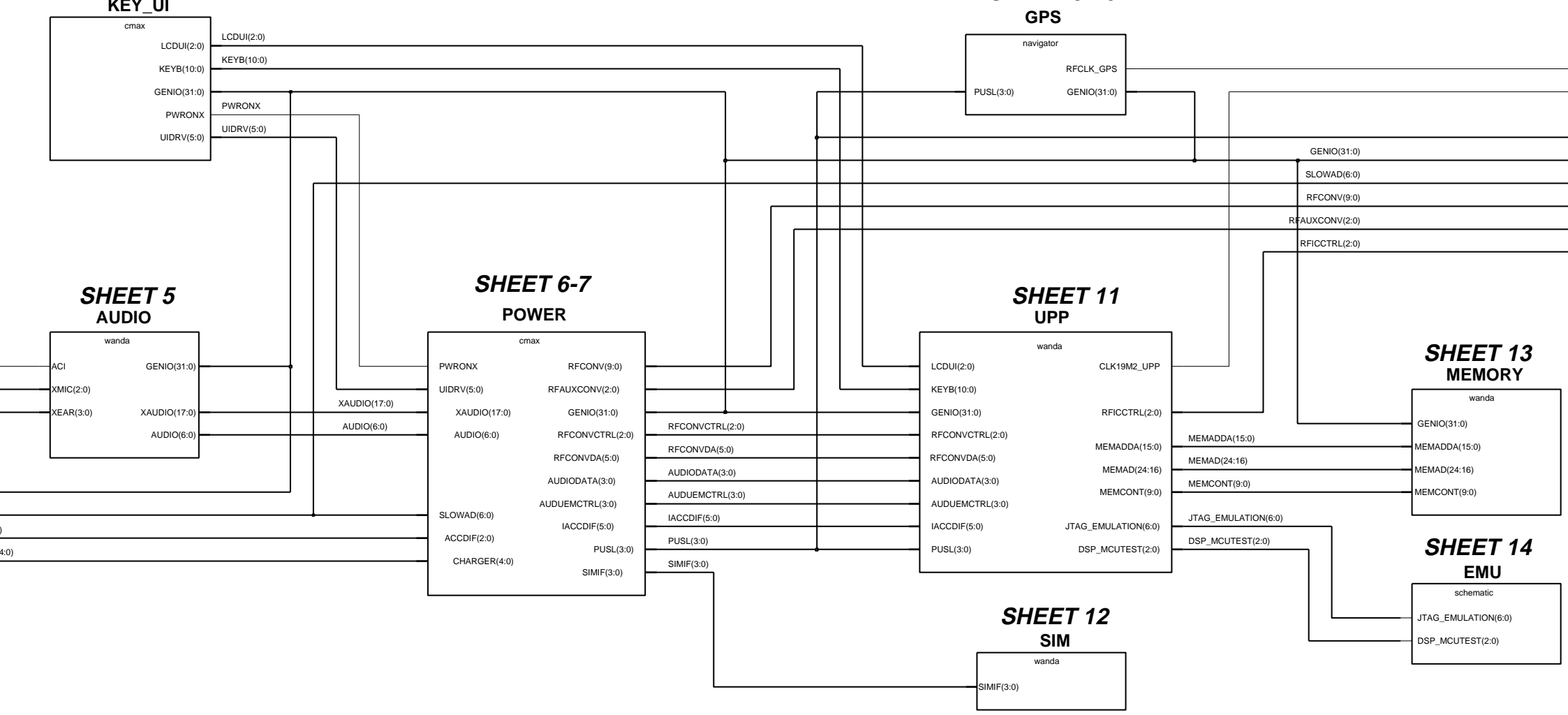
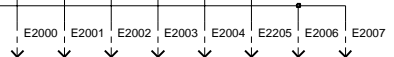
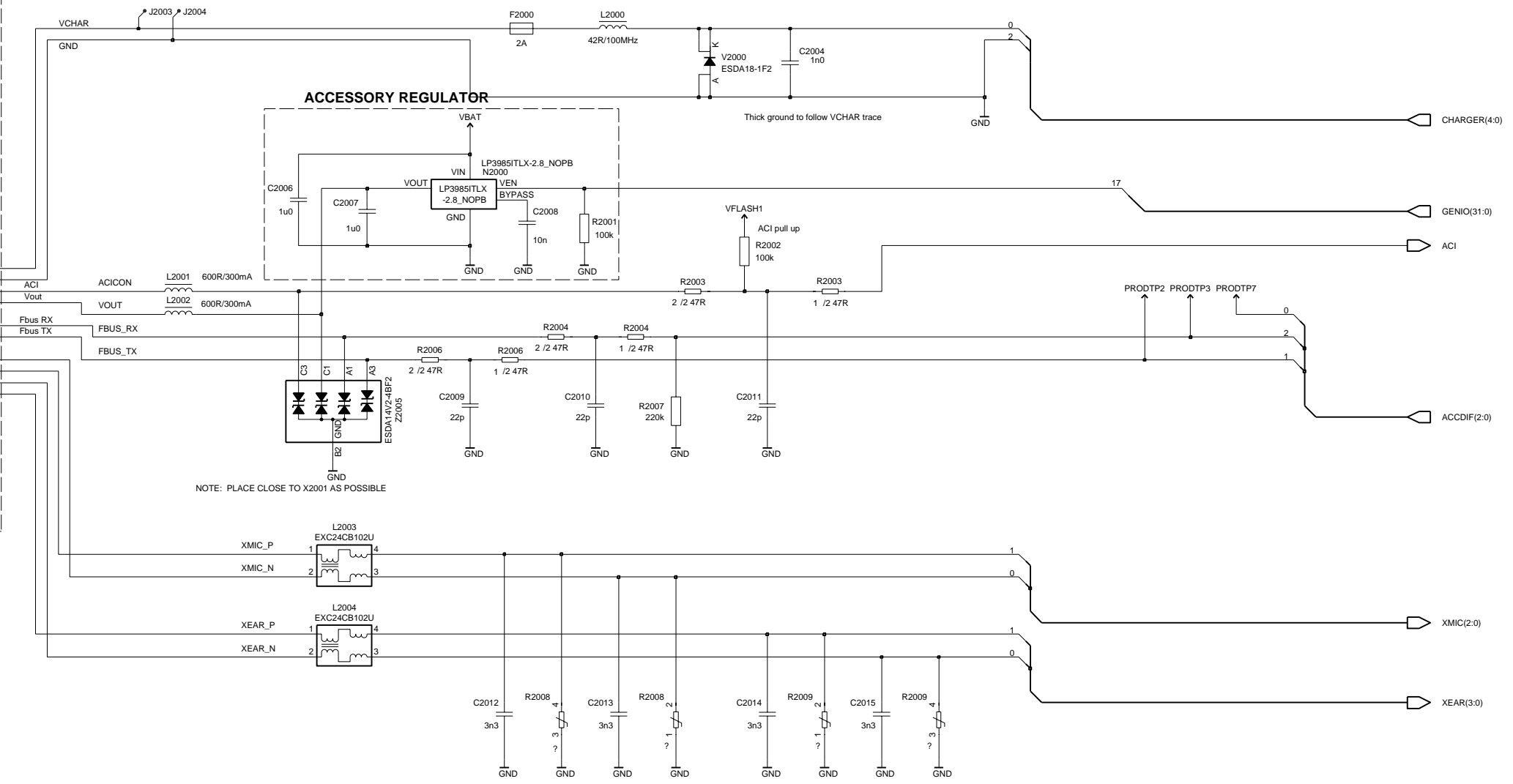


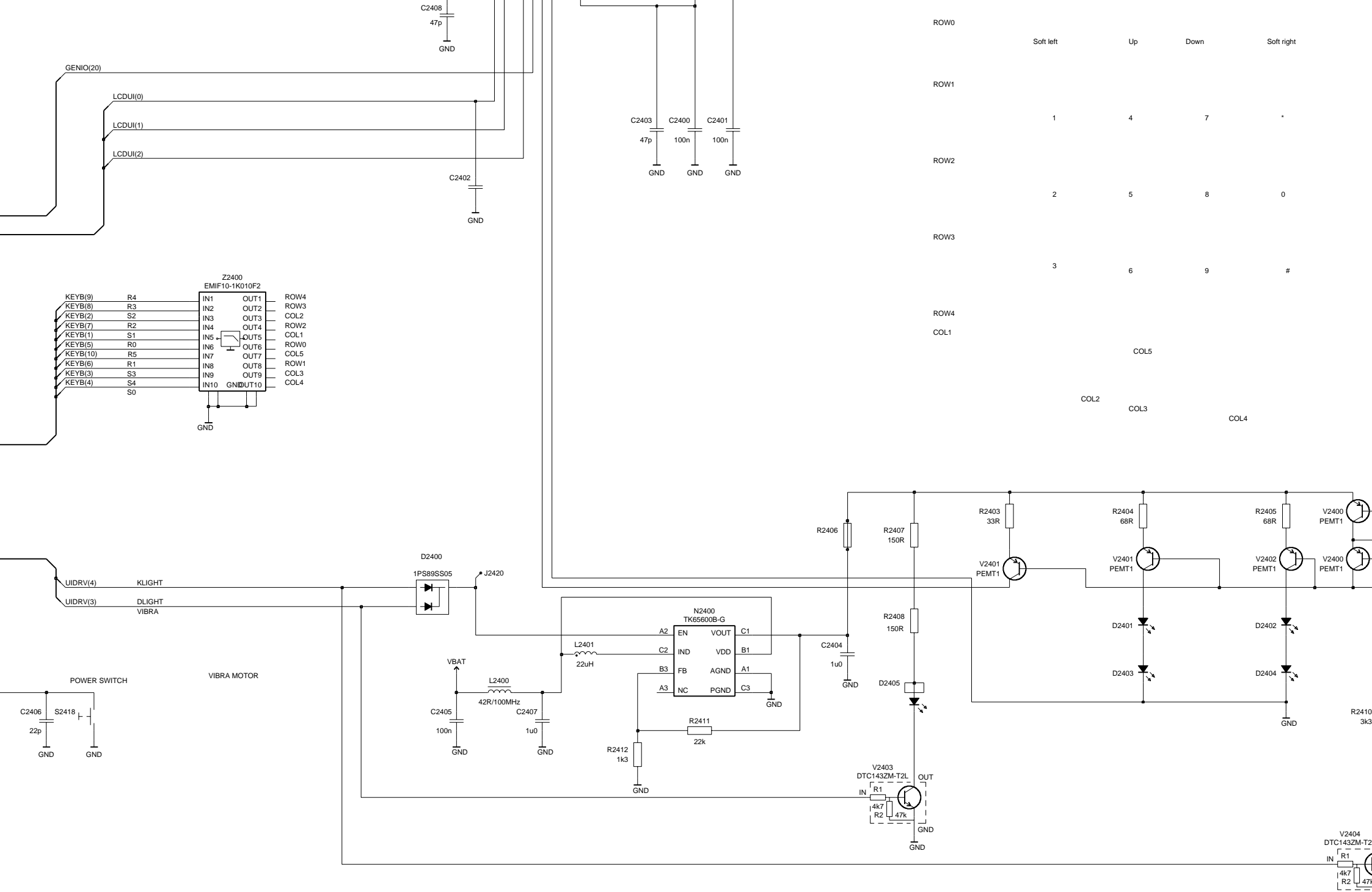
GENIO(31:0)	GENIO(31:0)	GENIO(31:0)	TX_GATE	TX_GATE	TX_GATE
			SYNTH_LE	SYNTH_LE	SYNTH_LE
			RX_IF_AGC	RX_IF_AGC	RX_IF_AGC
			TX_AGC2	TX_AGC2	TX_AGC2
			TX_AGC1	TX_AGC1	TX_AGC1
RFCONV(9:0)		RFCONV(9:0)	RX_IP	RX_IP	RX_IP
			RX_IN	RX_IN	RX_IN
			RX_QP	RX_QP	RX_QP
			RX_QN	RX_QN	RX_QN
			TX_IP	TX_IP	TX_IP
			TX_IN	TX_IN	TX_IN
			TX_QP	TX_QP	TX_QP
			TX_QN	TX_QN	TX_QN
			VREFRF	VREFRF	VREFRF01
RFAUXCONV(2:0)		RFAUXCONV(2:0)	AUXDAC	AUXDAC	PA_BIAS
			PWROUT	PWROUT	PWROUT
			AFC	AFC	AFC
RFICCTRL(2:0)		RFICCTRL(2:0)	RF_BUS_CLK	RF_BUS_CLK	RF_BUS_CLK
			RF_BUS_DATA	RF_BUS_DATA	RF_BUS_DATA
			RF_BUS_EN	RF_BUS_EN	RF_BUS_EN
SLOWAD(6:0)		SLOWAD(6:0)	FALSE_DET	FALSE_DET	FALSE_DET
			PA_TEMP	PA_TEMP	PA_TEMP
PUSL(3:0)	PUSL(3:0)	PUSL(3:0)	PURX	PURX	PURX
CLK19M2_UPP					CLK19M2_UPP
CLK19M2_GPS					CLK19M2_GPS



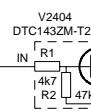


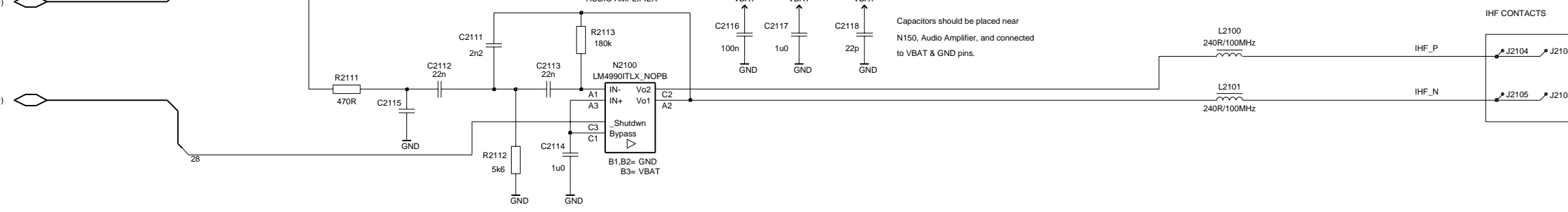
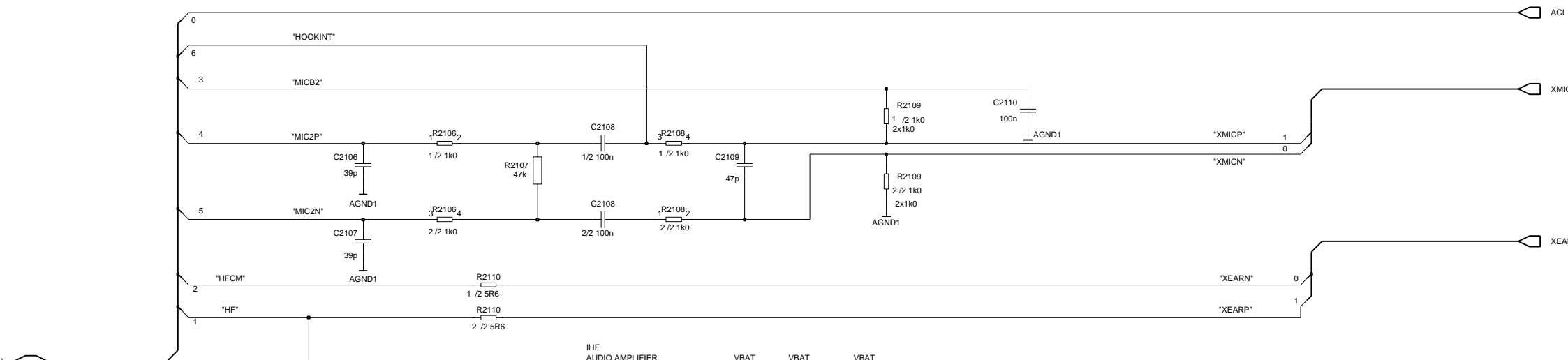
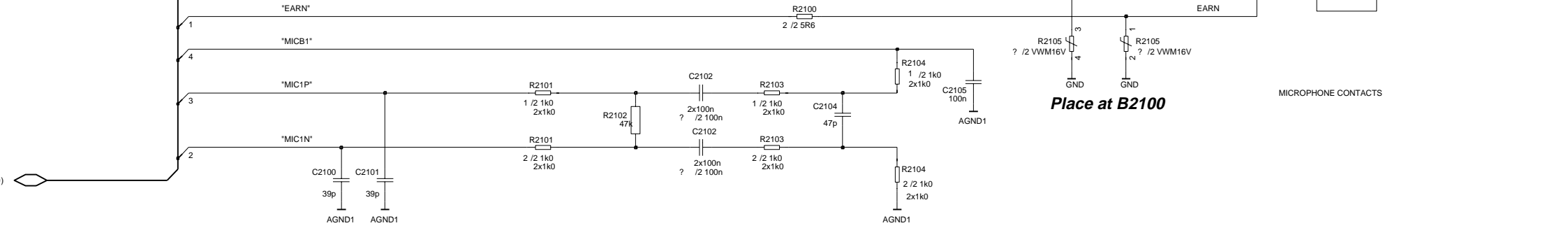
ACTOR

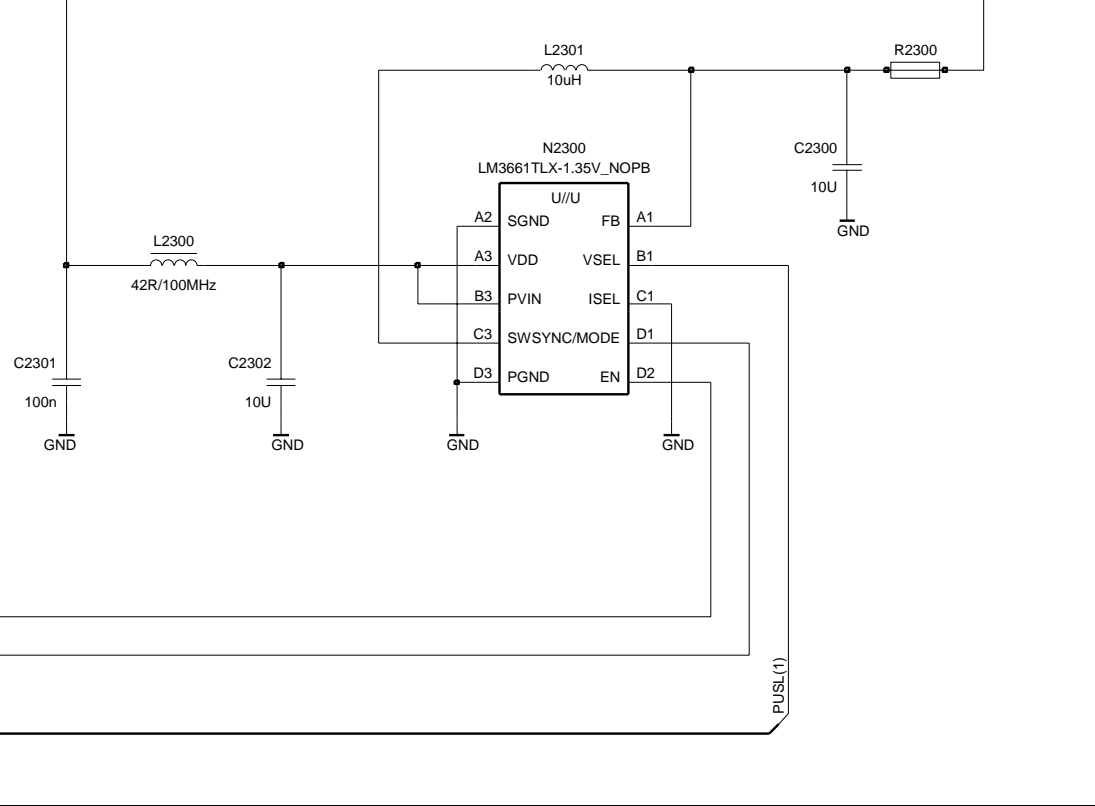


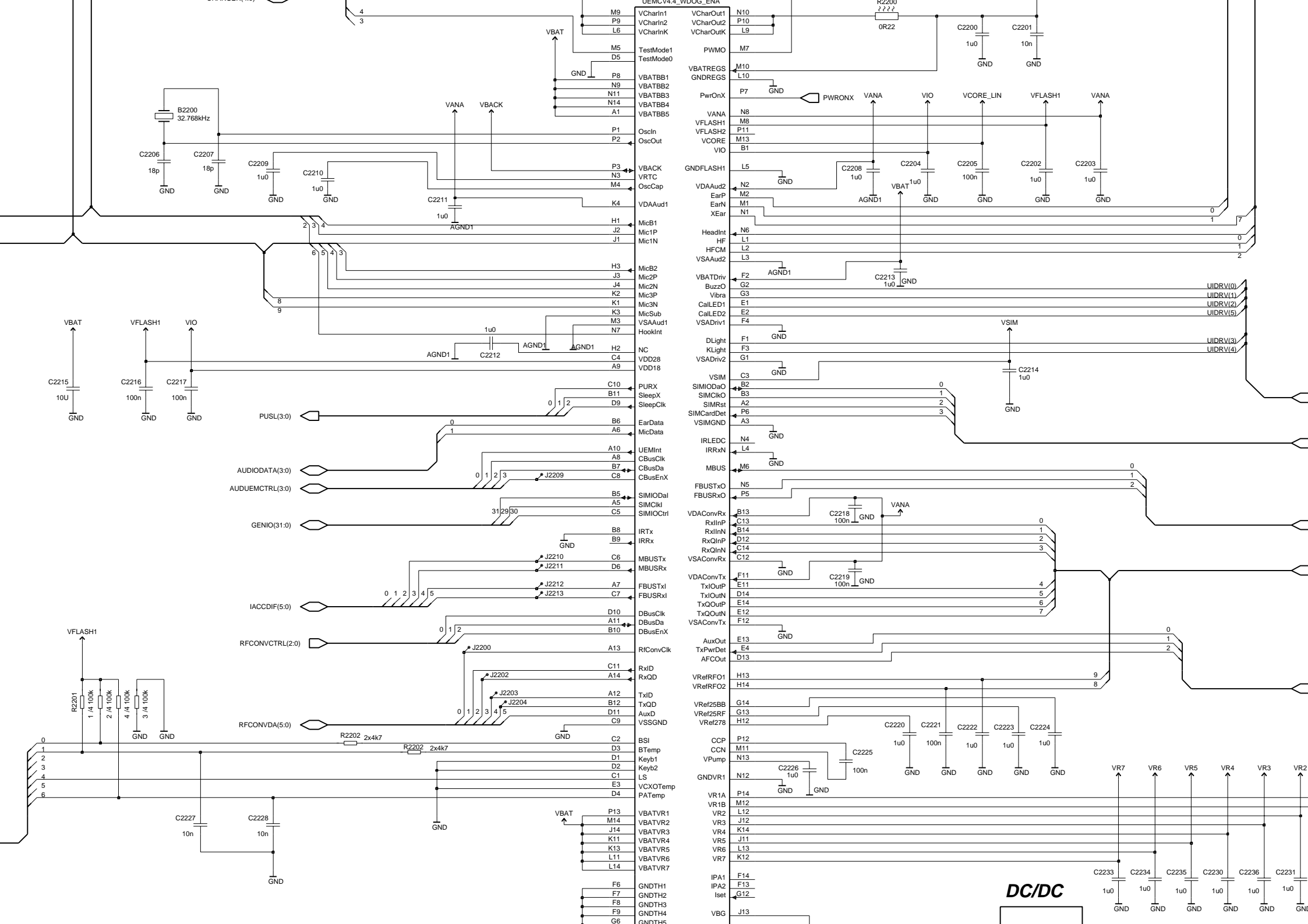


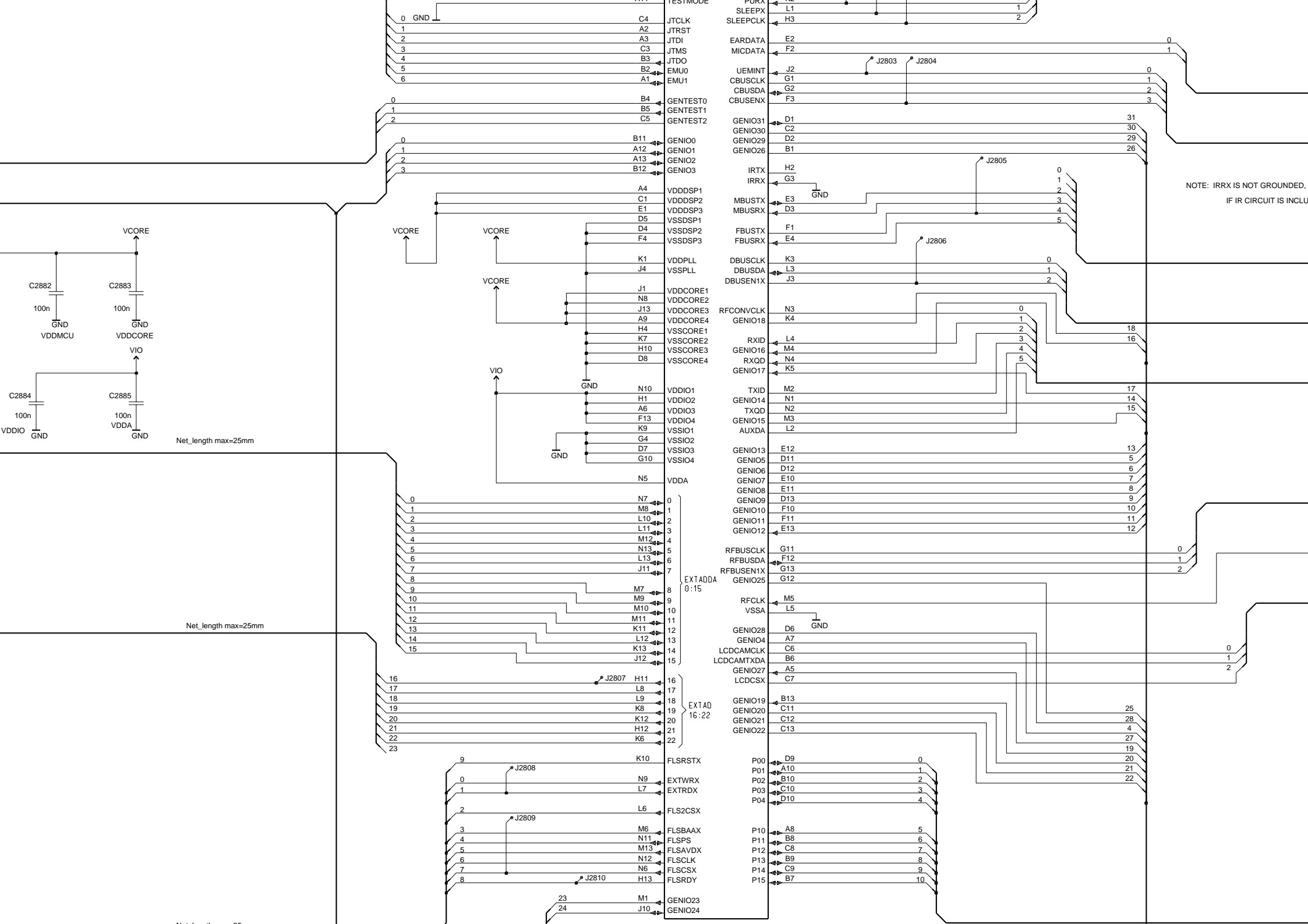
ROW	Soft left	Up	Down	Soft right
ROW1	1	4	7	*
ROW2	2	5	8	0
ROW3	3	6	9	#
ROW4				
COL1		COL5		
	COL2	COL3		COL4









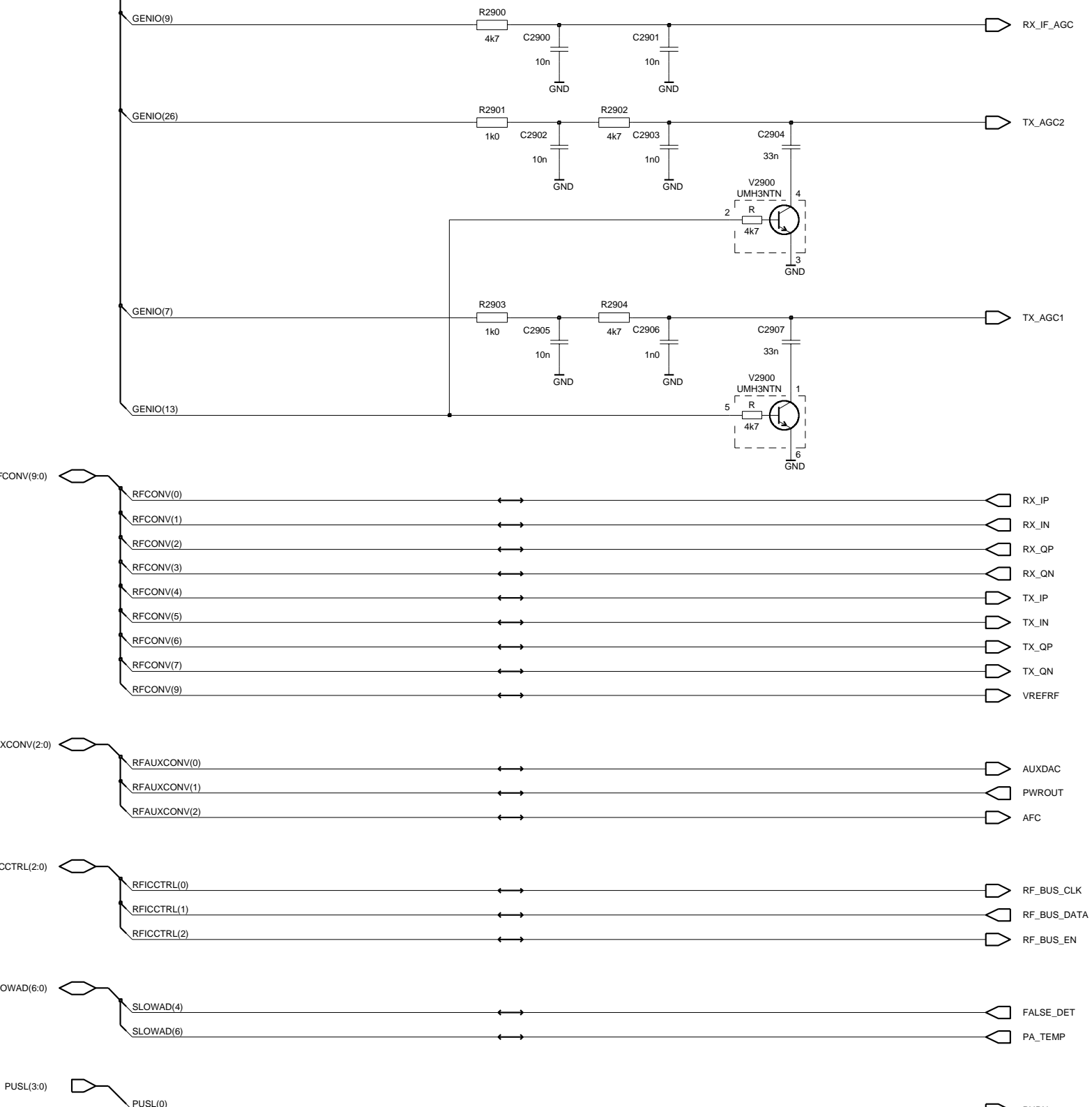


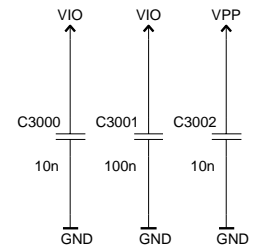
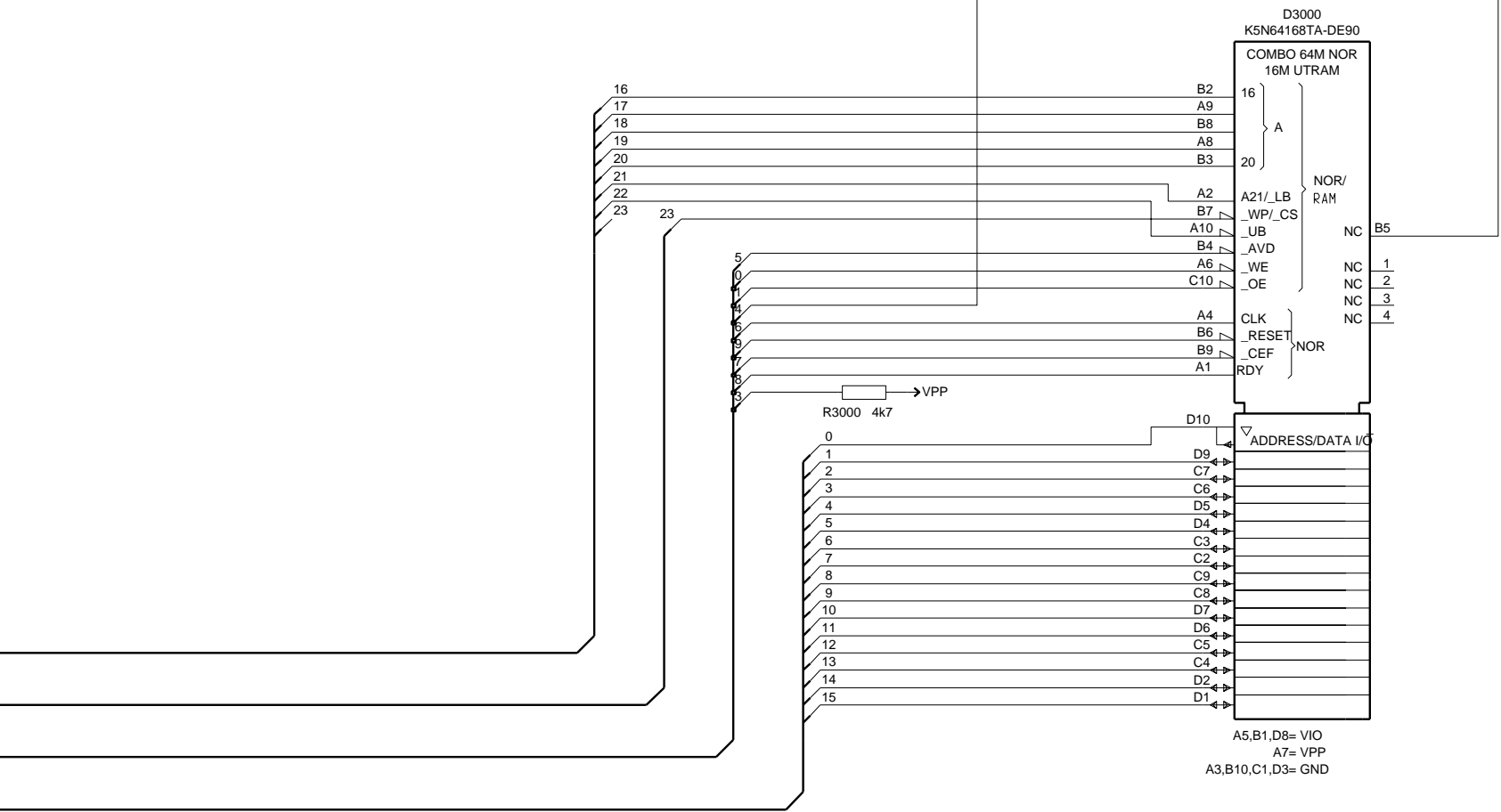
NOTE: IRRX IS NOT GROUNDED,
IF IR CIRCUIT IS INCLU...

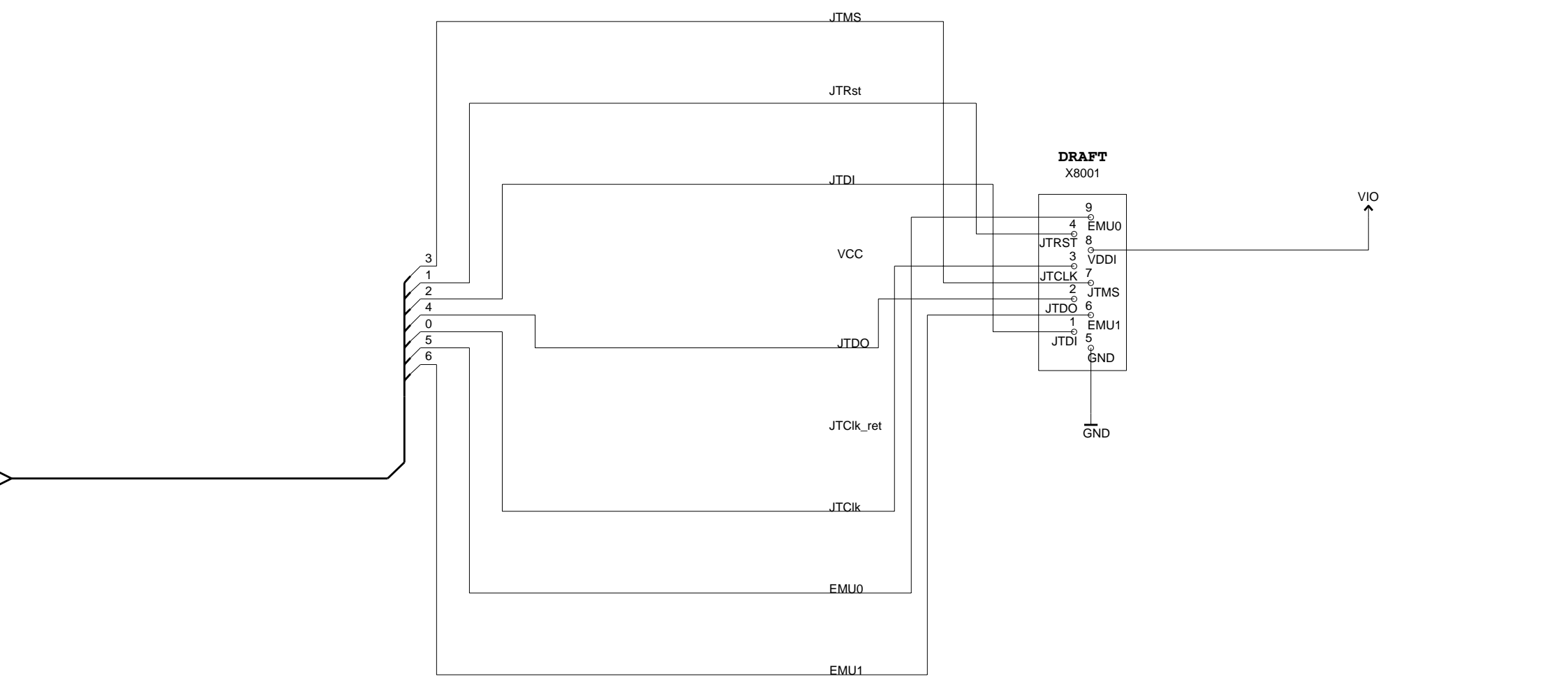
Net_length max=25mm

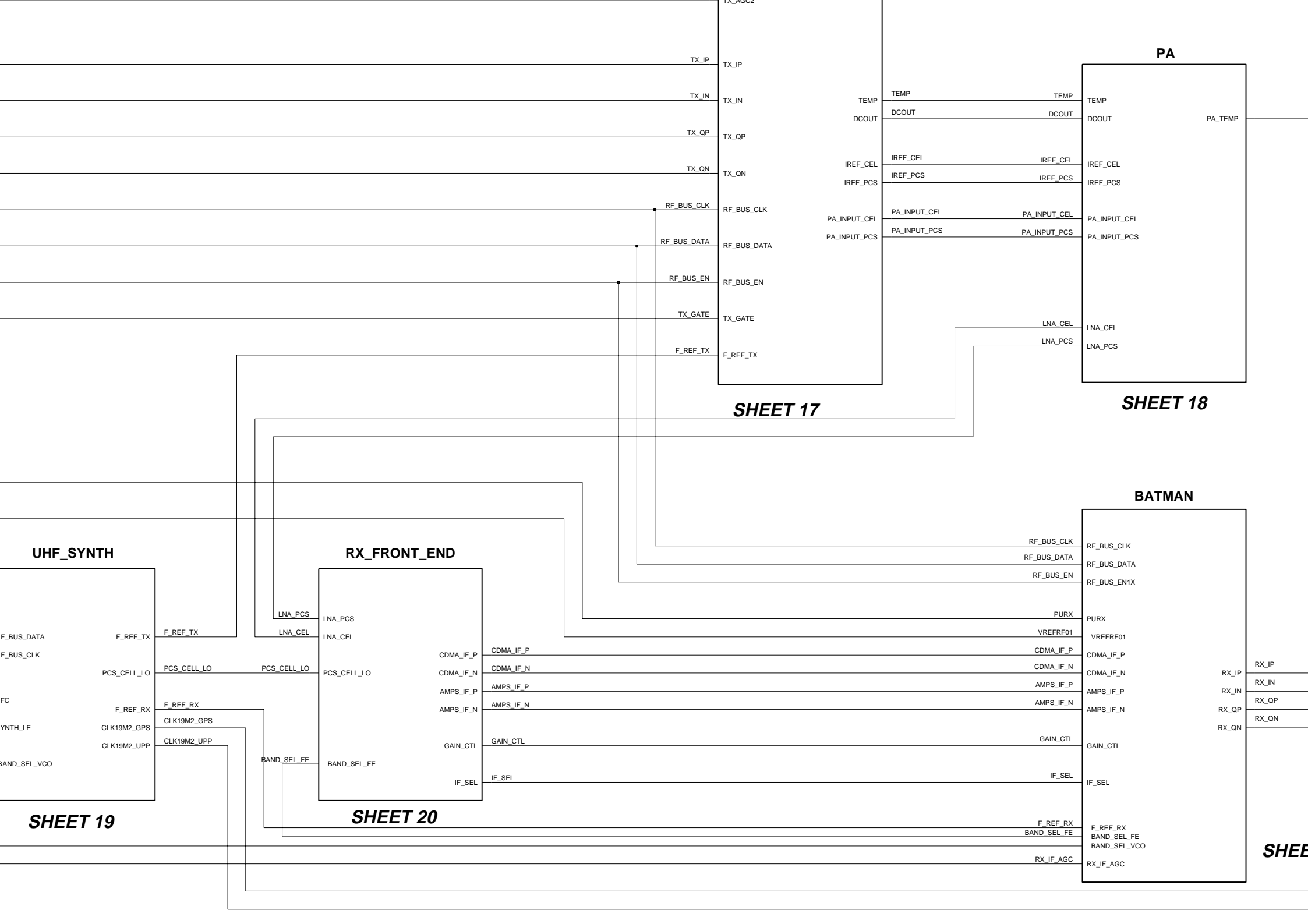
Net_length max=25mm

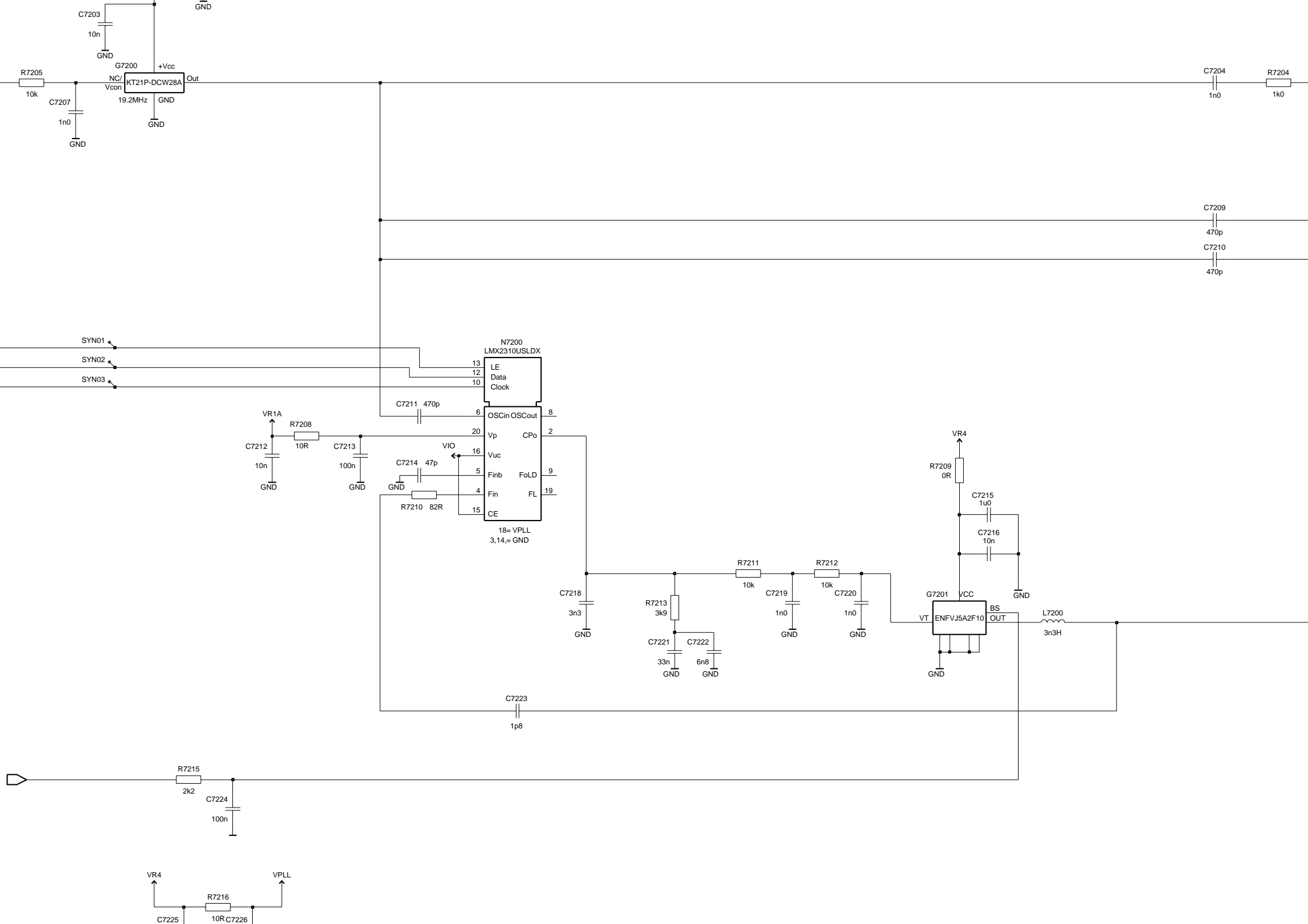
Net_length max=25mm

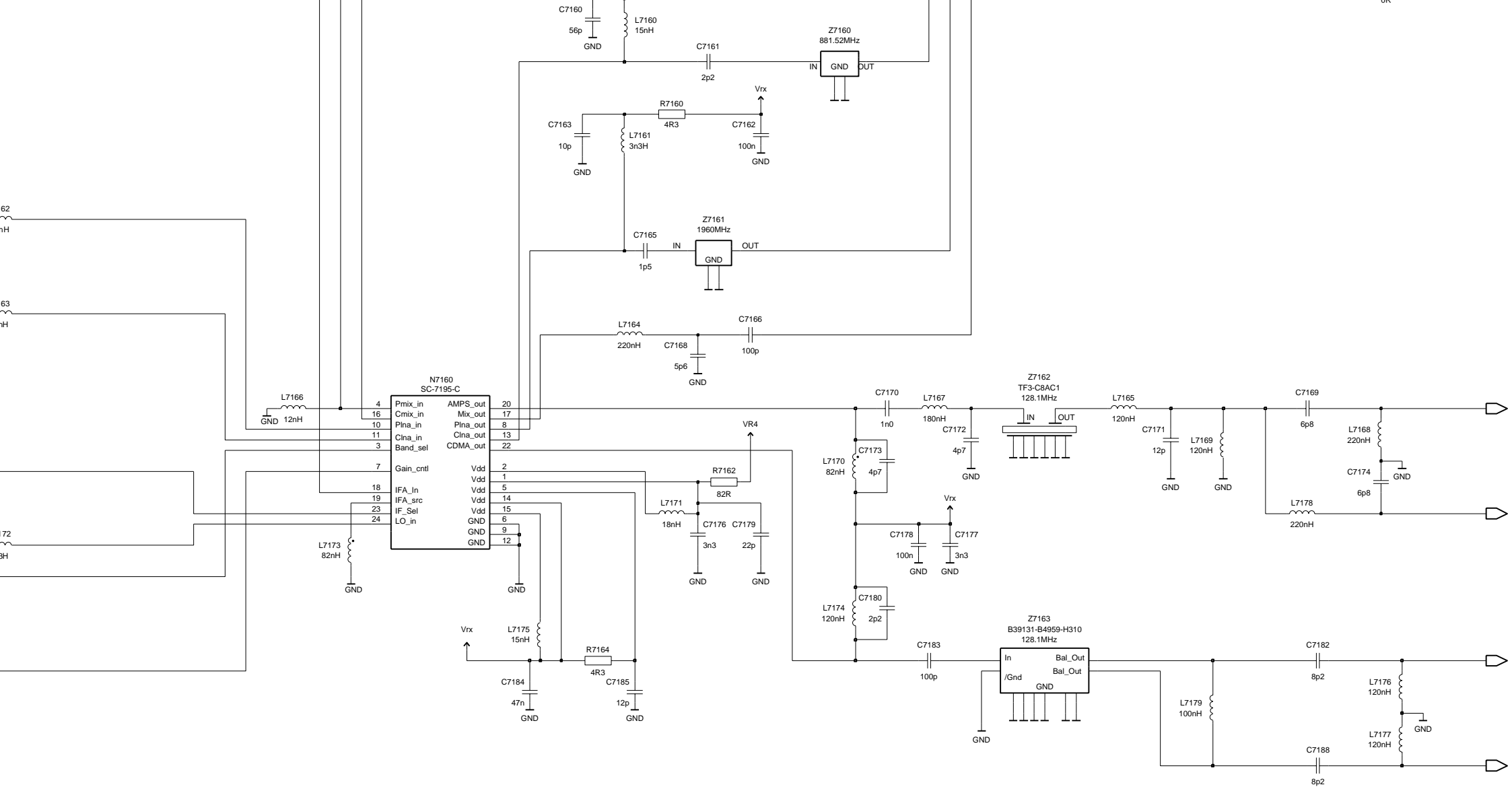






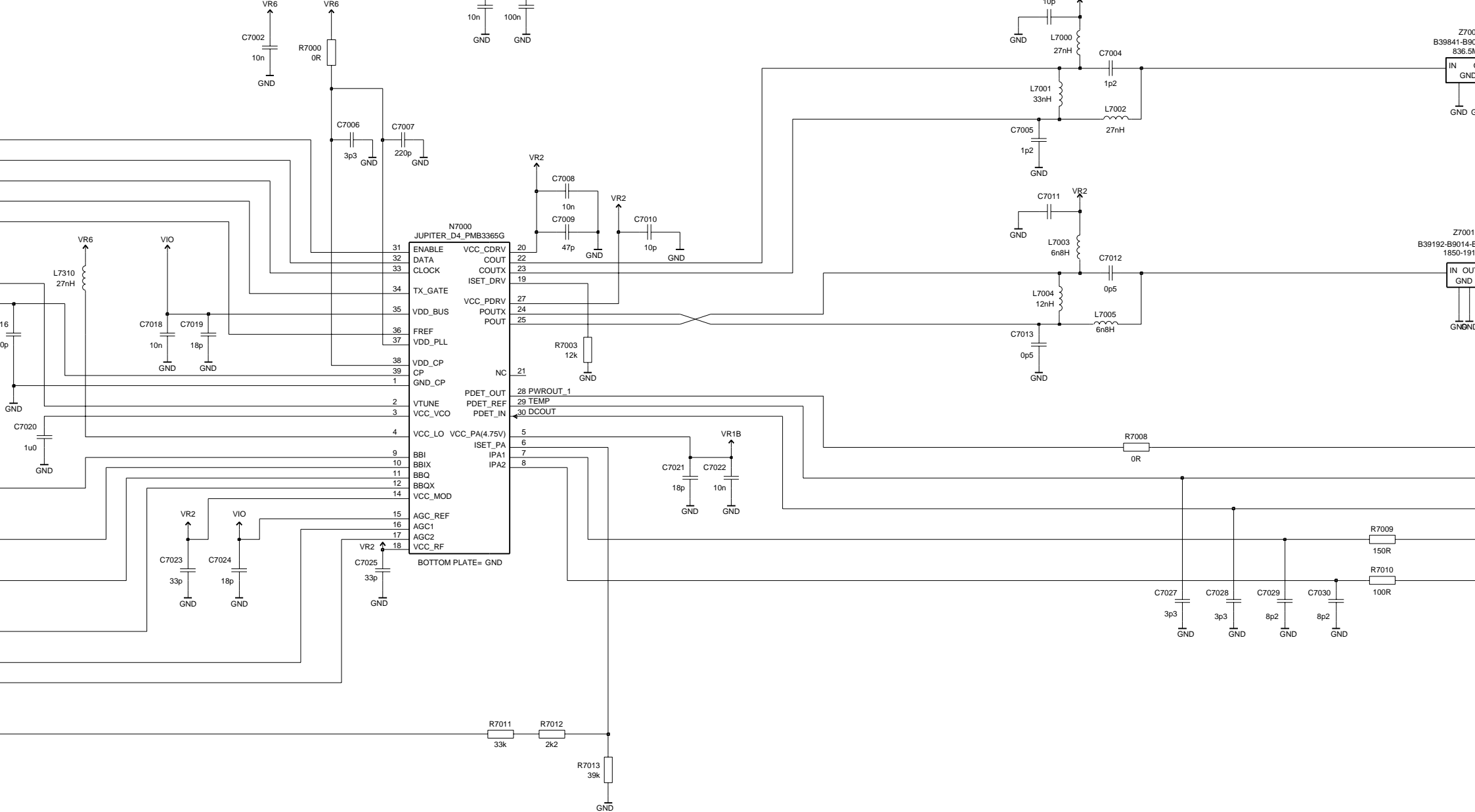


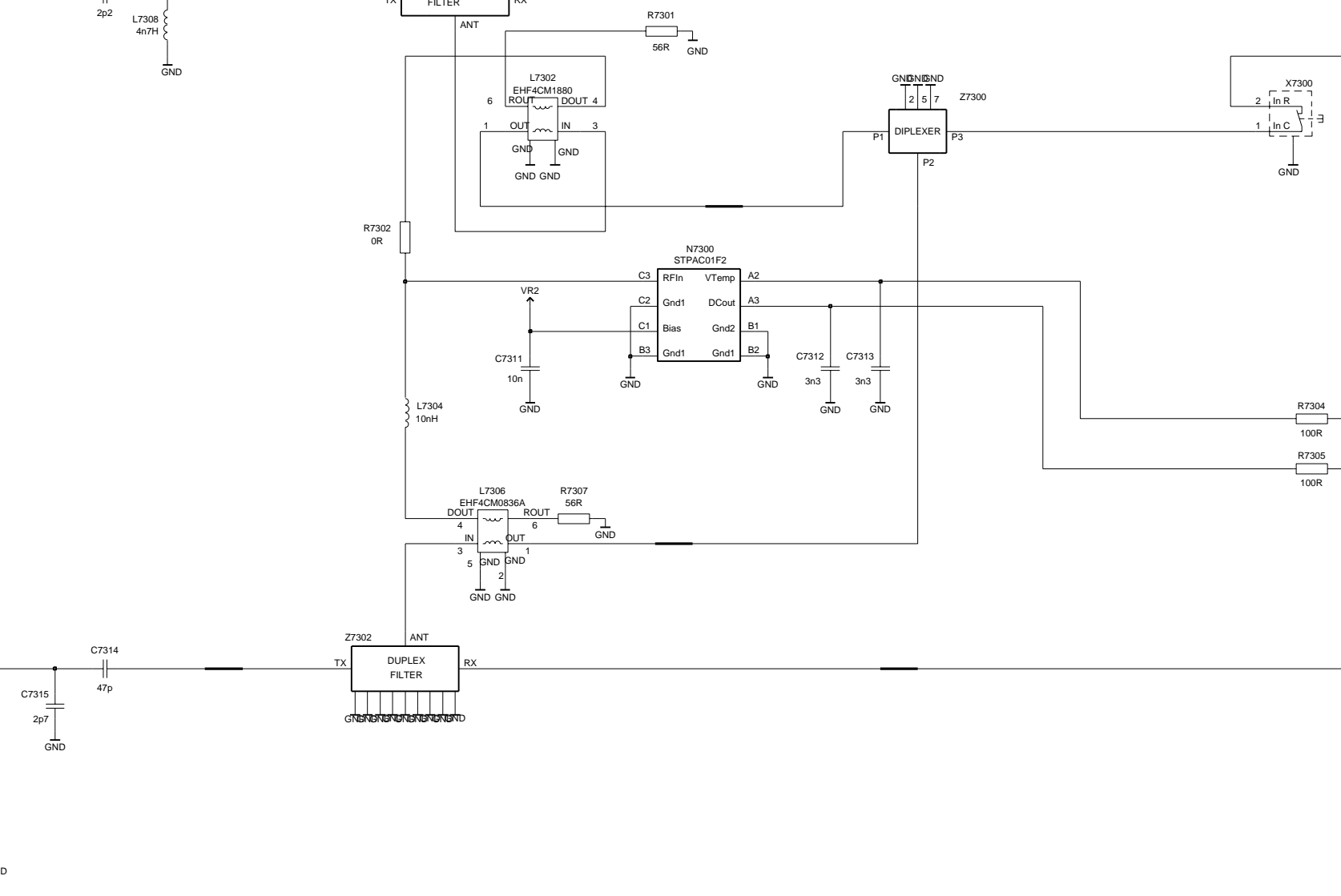
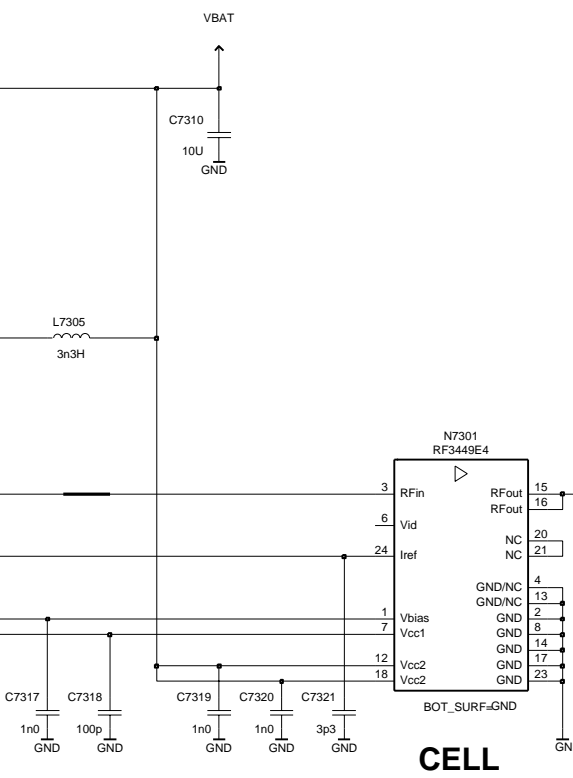
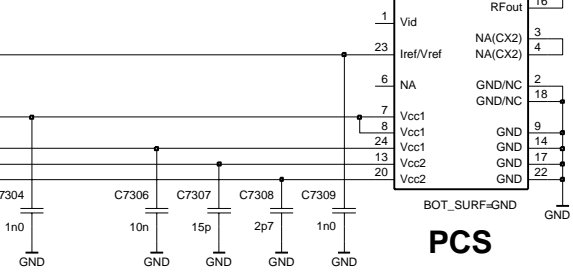


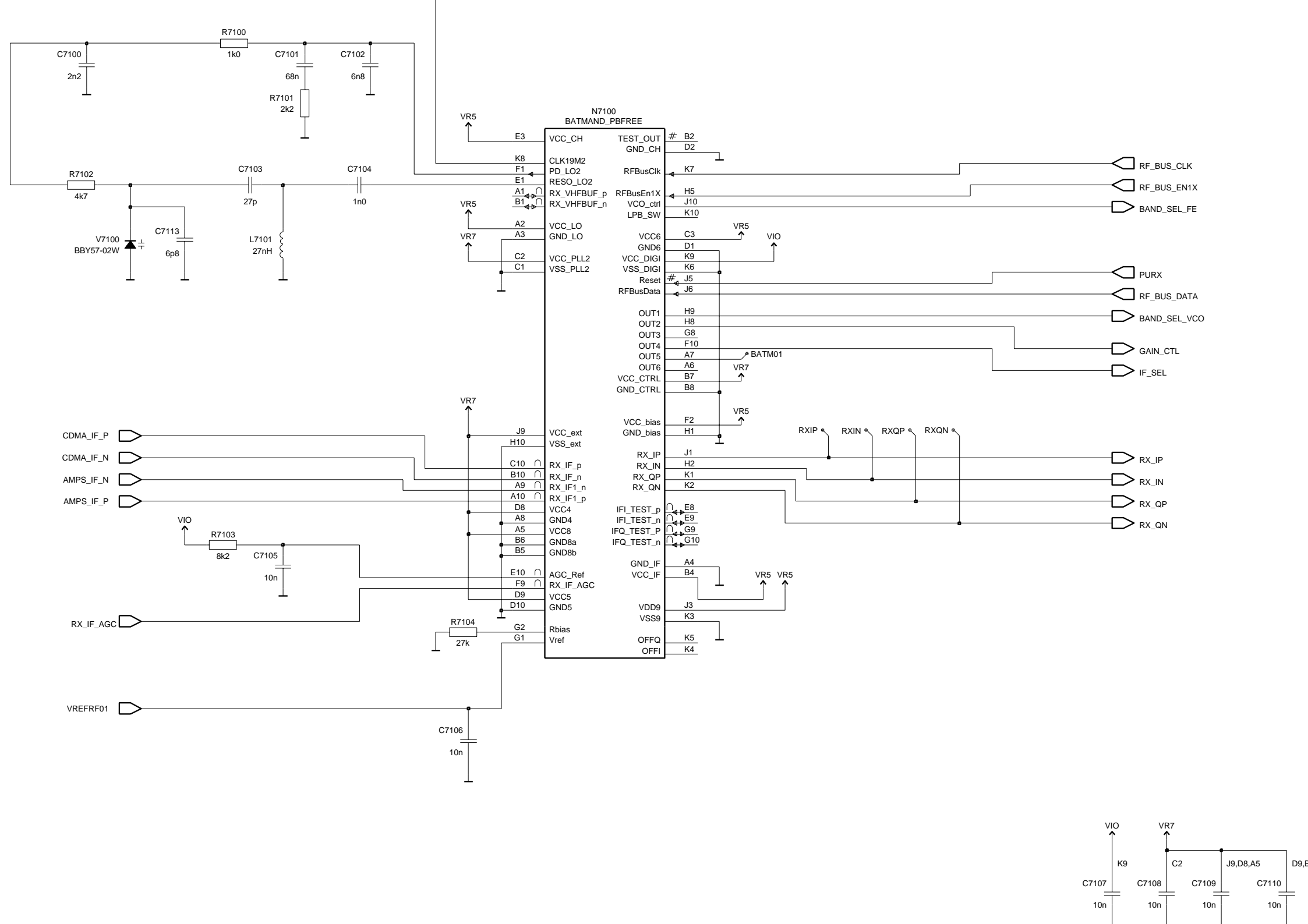


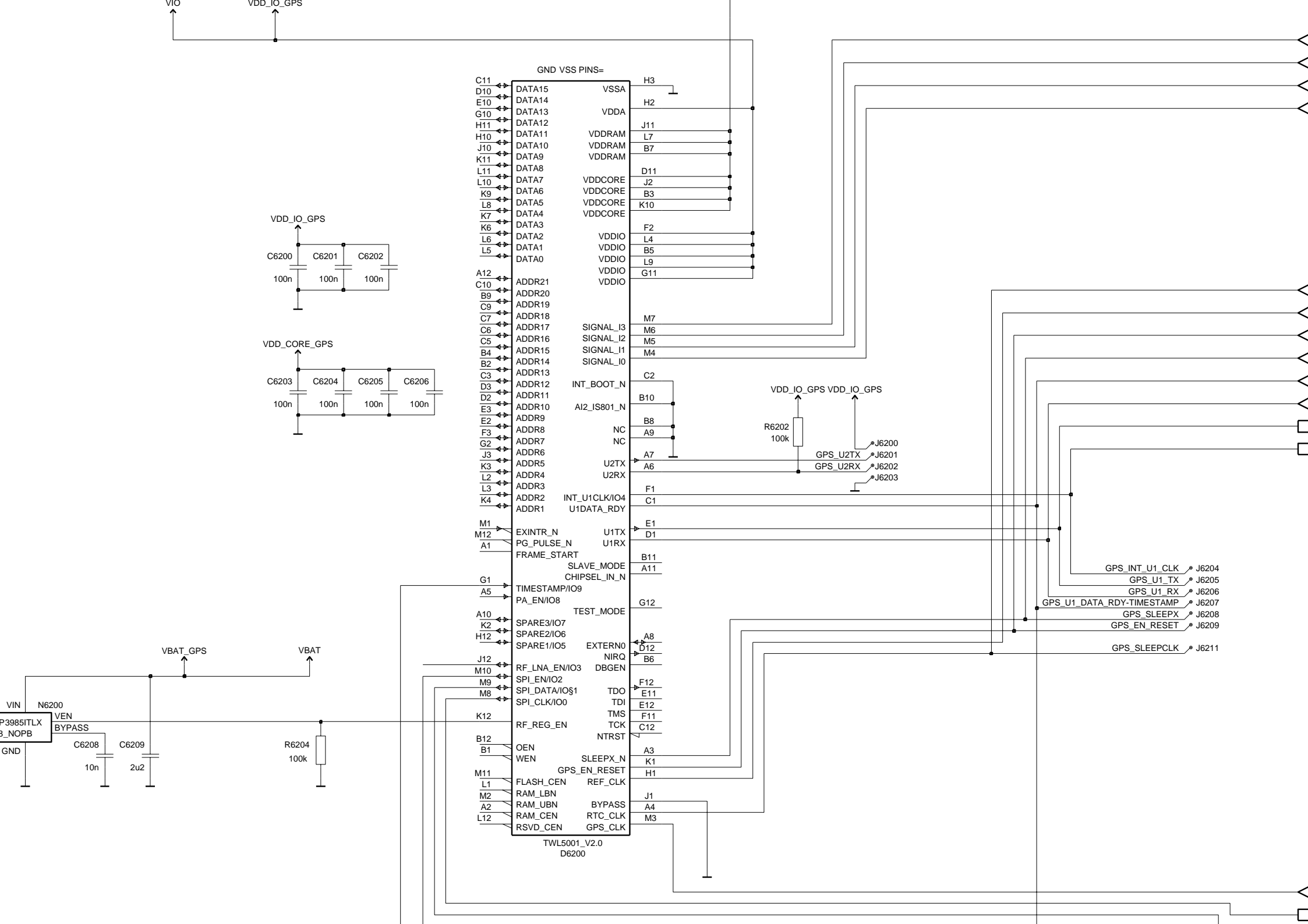
LOGIC INPUTS

BAND	GAIN_CTL	IF_SEL
0	1	0
0	0	0
1	1	0
1	0	0
0	1	1
0	0	1











C2400 0720

D2404

D2402

D2403

D2401



C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
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C2400

D2404

D2402

D2403

D2401



C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
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